NEURON® CHIP Special-Purpose Mode Transceiver Interface Specification

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Introduction

This document describes the interface between the NEURON CHIP and an attached transceiver when the NEURON CHIP communications port is configured to operate in special-purpose mode. This document does not cover the single-ended or differential modes of the NEURON CHIP. (See the section "Network Communications Port" in the *NEURON CHIP Advance Information*.)

Background

The special-purpose mode interface was designed to minimize the control lines between the NEURON CHIP and an intelligent transceiver. Characteristics of an intelligent transceiver include the following:

- Ability to configure various parameters of the transceiver from the NEURON CHIP
- Ability to report on various parameters of the transceiver to the the NEURON CHIP
- Multiple channel operation
- Multiple bit-rate operation
- Use of forward error correction
- Media-specific modulation techniques requiring special message headers and framing

In short, the special-purpose mode interface is designed to pass both network information as well as command and control information between the NEURON CHIP and the associated transceiver. This design minimizes the number of pins on each chip to achieve these functions and reduces the cost associated with the manufacture and testing.

A protocol between the two devices is used to deal with configuration and error reporting, as well as the passage of network data. This protocol consists of the NEURON CHIP and the transceiver each exchanging 8 bits of status and 8 bits of data simultaneously and continuously at rates up to 1.25 Mbps. The high data rate allows time-critical flags, such as carrier

detect, to be exchanged across the interface with network data rates up to 156 Kbps.

Because the NEURON CHIP communication firmware is the same in all NEURON CHIP-based devices, a further requirement exists that the interface be general enough to support future transceiver development with existing NEURON CHIP firmware. This is accomplished by writing a fixed amount of configuration information from the NEURON CHIP to the transceiver, and by reading a fixed amount of status information from the transceiver to the NEURON CHIP. All NEURON CHIPs have some amount of EEPROM on them that is initialized with the configuration information necessary to initialize the associated transceiver. Upon receipt of a network management message, the NEURON CHIP firmware can read the status registers within the transceiver and report their contents to a requesting device for network debugging and analysis. The NEURON CHIP firmware does not know what the status indicates; it is assumed that the application program requesting the status information is able to understand it.

Special-Purpose Mode Physical I/O

When the NEURON CHIP is configured to operate in special-purpose mode, the NEURON CHIP and transceiver exchange status and data over a synchronous serial bus on pins CP0, CP1, CP2, CP4.

CP0 (RX input) is the serial link from the transceiver to the NEURON CHIP. During each frame period, eight bits of status and eight bits of data are sent from the transceiver to the NEURON CHIP.

CP1 (TX output) is the serial link from the NEURON CHIP to the transceiver. During each frame period, eight bits of status and eight bits of data are sent from the NEURON CHIP to the transceiver.

CP2 (BIT clock output) is a bit clock generated by the NEURON CHIP that clocks data and status in and out of the NEURON CHIP and transceiver. The falling edge of BIT clock output is used by the NEURON CHIP to clock in RX input and to clock out TX output. The rate of the bit clock is the same as that of the communication port clock on the NEURON CHIP. The communication port clock rate is related to the NEURON CHIP input clock rate; for special-purpose mode, the communication port clock should be configured to either ÷8 or ÷16 of the NEURON CHIP input clock. It is recommended that the communication port clock be at least 8 times as fast as the data rate on the communication medium.

CP4 (Frame clock output) is a frame clock generated by the NEURON CHIP that pulses high for one bit time every 16 bit times on the serial link. The

frame clock establishes a period of 16 bits during which eight bits of status and eight bits of data are exchanged.

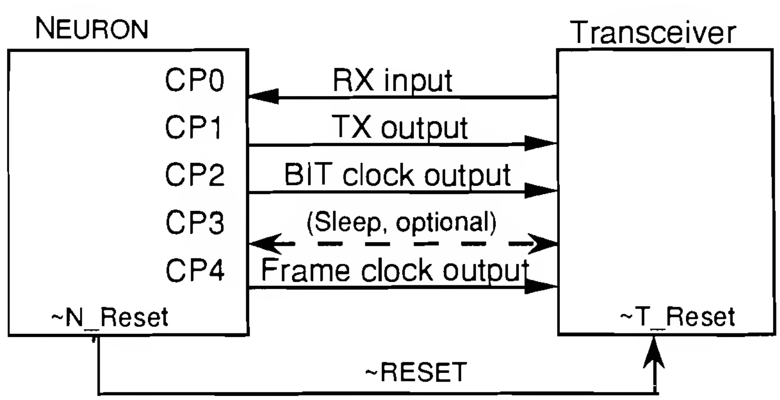
Figure 1 shows the communication port I/O and their timing relations in special-purpose mode.

The fifth I/O pin, CP3, of the communication port is defined as Sleep. Support of this pin's function is optional on the transceiver. When the pin is connected to a transceiver with sleep capability, the NEURON CHIP can be configured to operate in one of two ways:

1) The NEURON CHIP can be configured so that any incoming message will wake it up. In this case, CP3 is an input to the NEURON CHIP.

2) The application program running on the NEURON CHIP can decide to sleep periodically and assert the pin low. In this case, the pin is an output. This will cause the transceiver to power down whenever the NEURON CHIP application program instructs the NEURON CHIP, and any device connected to the Sleep output pin, to go to sleep. When the Sleep pin is high, the transceiver is to be awake; when it is low, it is assumed that the transceiver is asleep.

The transceiver also has a Reset input that is tied to the NEURON CHIP's Reset input. The transceiver resets its state and internal registers when this input is active. The transceiver must not cause the NEURON CHIP to be reset by asserting this line.



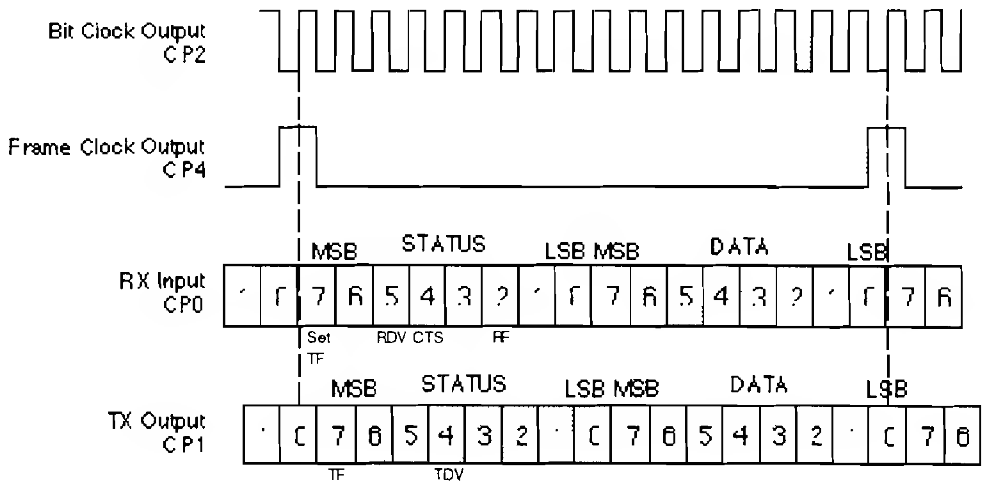


Figure 1. Comm port I/O and special-purpose mode data format

Status Bits

The eight-bit status field sent from the NEURON CHIP to the transceiver on CP1 (TX output) is denoted TX.ST. The eight-bit status field sent from the transceiver to the NEURON CHIP on CP0 (RX) is denoted RX.ST. The individual bits in each of the status fields are named as follows.

TX Output, Status Bits (TX.ST)

bit 7	TX_FLAG	NEURON CHIP in the process of transmitting packet
bit 6	TX_REQ_FLAG	NEURON CHIP requests to transmit on the network
bit 5	TX_DATA_VALID	NEURON CHIP is passing network data to the transceiver in this frame
bit 4	Don't Care	Zero
bit 3	TX_ADDR_R/W	NEURON CHIP is writing internal transceiver register
bit 2	TX_ADDR_2	Address bit 2 of internal transceiver register (1 .. 7) *
bit1	TX_ADDR_1	Address bit 1 of internal transceiver register (1 .. 7) *
bit 0	TX_ADDR_0	Address bit 0 of internal transceiver register (1 .. 7) *

RX Input, Status Bits (RX.ST)

bit 7	SET_TX_FLAG	Transceiver accepts request to transmit packet
bit 6	CLR_TX_REQ_FLAG	Transceiver acknowledges request to transmit packet
bit 5	RX_DATA_VALID	Transceiver is passing network data to the NEURON CHIP in this frame
bit 4	TX_DATA_CTS	Transceiver indicates to the NEURON CHIP that it is clear to send byte of network data to the transceiver
bit 3	SET_COLL_DET	Transceiver indicates that it has detected a collision while transmitting the preamble
bit 2	RX_FLAG	Transceiver has detected a packet on the network
bit 1	RD/WR_ACK	Transceiver acknowledges read/write to internal register
bit 0	TX_ON	Transceiver is transmitting on the network

* Note that internal transceiver Register 0 is not defined. Registers 1 through 7 are defined by the transceiver implementation. A write of register 0 is the steady-state condition.

Table 1. Special-purpose mode transmit and receive status bits

The definitions of the status bits are described first in the text below. Following the text is a series of diagrams illustrating the status bits exchanged between the NEURON CHIP and transceiver and an example state diagram for the transceiver.

Transmit Sequences

In order to request to transmit on the network, the NEURON CHIP sets a latch whose output is TX_REQ_FLAG (TX.ST bit 6). This latch on the NEURON CHIP is cleared by the transceiver via CLR_TX_REQ_FLAG (RX.ST bit 6), which is asserted by the transceiver for one frame only. In the same frame as CLR_TX_REQ_FLAG is asserted, the transceiver either accepts or

rejects the request for transmission. The transceiver accepts the request by asserting SET_TX_FLAG (RX.ST bit 7) for one frame only. The transceiver rejects the request by NOT asserting SET_TX_FLAG in the frame. If the transceiver accepts the request for transmission, the transceiver must also assert TX_DATA_CTS (RX.ST bit 4) in the *same* frame as CLR_TX_REQ_FLAG and SET_TX_FLAG, indicating that the NEURON CHIP may send the first byte of data.

In the case where the transceiver accepts the request for transmission and asserts SET_TX_FLAG for one frame, a latch on the NEURON CHIP whose output is TX_FLAG (TX.ST bit 7) is set. This latch is cleared by the NEURON CHIP to end transmission. In addition, the transceiver sets TX_ON (RX.ST bit 0) high, which indicates it is transmitting on the network.

The transceiver looks for the carrier signal on the network right up until it either accepts or rejects the request for transmission. With each transceiver checking to ensure the network is idle immediately before accepting the request and beginning to transmit, the occurrence of collisions on the network is minimized and thus performance is improved. If the transceiver sees carrier on the network, it rejects the request to transmit by setting CLR_TX_REQ_FLAG only for one frame. (Refer to "Receive Sequences" below for the transceiver's following response to carrier.) If the transceiver sees no carrier on the network, it accepts the request by setting CLR_TX_REQ_FLAG, SET_TX_FLAG, and TX_DATA_CTS for one frame and immediately begins transmitting the preamble on the network, as described below.

When a transceiver accepts the request for transmission, it begins to send its preamble on the network. The content of the preamble is defined by the transceiver. The NEURON CHIP imposes a minimum requirement on the duration of preamble such that a receiving NEURON CHIP has sufficient time between being informed of an incoming packet and actual reception of incoming bytes. For more information, see the section "NEURON CHIP Handshake Timing." On reception the transceiver strips off the preamble and returns only valid data bytes to the NEURON CHIP.

To send a byte of data, the NEURON CHIP shifts eight bits out in the field TX.DATA bits 7-0. (Bit 7 is the MSB and is shifted out first.) In the same frame as the data is shifted out, the NEURON CHIP asserts TX_DATA_VALID for one frame only. (Note: The status field TX.ST precedes TX.DATA in each frame such that TX_DATA_VALID is asserted before TX.DATA is shifted out.) The NEURON CHIP may set the first TX_DATA_VALID in the first frame in which TX_FLAG is set.

The NEURON CHIP may not send another byte of data to the transceiver until the transceiver indicates it is ready by asserting TX_DATA_CTS for one frame only, after which the NEURON CHIP may send another byte. This is repeated for each byte. During this time, the NEURON CHIP maintains TX_FLAG set and the transceiver maintains TX_ON set.

After the NEURON CHIP has sent the last byte of data, it clears TX_FLAG to indicate end of transmission. At any time, if the NEURON CHIP wants to abort transmission, it clears TX_FLAG. The transceiver transmits the last bytes of data and then stops transmitting. When the transceiver has completed transmitting the packet on the medium, it clears TX_ON.

TX_FLAG must be cleared by the NEURON CHIP at least one frame following the last assertion of TX_DATA_VALID. The NEURON CHIP does not need TX_DATA_CTS to be asserted after it sends the last byte of data before it may clear TX_FLAG. The NEURON CHIP may cause an extra TX_DATA_VALID to be asserted after TX_FLAG has been reset. This TX_DATA_VALID, asserted when TX_FLAG is low, must be ignored.

TX_ON (RX.ST bit 0) reports the state of the transceiver's transmitter to the NEURON CHIP. The NEURON CHIP's firmware watches this bit after it resets TX_FLAG. This bit is used for synchronization of the network by the protocol. In addition, if this flag fails to clear, the NEURON CHIP will reset the transceiver in an attempt to turn the transmitter off. The reset occurs as a result of a watchdog timer reset on the NEURON CHIP.

The amount of buffering on the transceiver must be enough such that the transceiver does not have an underflow condition. (That is, the transceiver needs another byte of data to transmit or an indication to stop transmitting, but does not receive it in time.) In case of underflow, the transceiver sends all zeros on the network. The maximum time between the assertion of TX_DATA_CTS by the transceiver and the assertion of TX_DATA_VALID by the NEURON CHIP is specified in the section "NEURON CHIP Handshake Timing." Also, the maximum time after the final TX_DATA_VALID until TX_FLAG is cleared is specified in the handshake timing section.

If the transceiver detects a collision while transmitting the preamble, it asserts SET_COLL_DET (RX.ST bit 3) for one frame. The earliest that SET_COLL_DET may be asserted by the transceiver is in the frame following SET_TX_FLAG. (Not all transceivers support collision detection; if a transceiver does not, the bit SET_COLL_DET must remain low.) SET_COLL_DET clears the latch on the NEURON CHIP whose output is TX_FLAG, thus aborting transmission. SET_COLL_DET also sets a latch on

the NEURON CHIP that indicates to one of the CPUs that there was a collision.

Receive Sequences

When the transceiver detects a carrier signal on the medium, it attempts to establish with a high level of certainty that the carrier detect indication is indeed an incoming packet and not a false carrier detect indication. When the transceiver establishes that there is an incoming packet, it sets a latch whose output is RX_FLAG (RX.ST bit 2).

Note that the transceiver uses two separate indications: one for carrier detect and one for incoming packet. As described in "Transmit Sequences" previously, in order to avoid collisions, the carrier detect indication causes the transceiver to reject a concurrent request for transmission. However, in order not to falsely indicate to the NEURON CHIP that a packet is incoming, the transceiver processes the signal for some duration to establish with a high level of certainty that there is an incoming packet before setting RX_FLAG. This may involve processing carrier sync, bit sync, or word sync.

After setting RX_FLAG, the transceiver strips off the preamble and returns only valid data bytes to the NEURON CHIP. When the transceiver receives the first byte of data, it shifts eight bits out in the field RX.DATA bits 7-0. (Bit 7 is the MSB and is shifted out first.) In the same frame, the transceiver asserts RX_DATA_VALID (RX.ST bit 5) for one frame only. (Note: The status field RX.ST precedes RX.DATA in each frame such that RX_DATA_VALID is asserted before RX.DATA is shifted out.) Each subsequent byte is sent to the NEURON CHIP in the same way with no handshaking from the NEURON CHIP. Note: RX_FLAG must be set at least one frame before the first RX_DATA_VALID.

After the transceiver has detected the end of a packet and delivered the final byte of data to the NEURON CHIP, it clears RX_FLAG. The transceiver must not deliver trailing bits of invalid data to the NEURON CHIP. (This implies that the transceiver must account for any delay in detecting the end of carrier and any padding with zeros for error coding not done on byte-size blocks.) If the transceiver needs to abort the receive sequence for some reason (e.g. no bit sync, no word sync), it clears RX_FLAG.

Configuration Command and Status Request Sequences

A NEURON CHIP CPU writes to seven 8-bit registers on the transceiver and reads seven 8-bit registers on the transceiver. The definition of the contents of these registers is specific to each transceiver. However,

every transceiver must have at least one configuration register containing at least one configuration bit. The required bit is bit 7 of Configuration Register 1. The function of this bit is described under "Configuration Command."

TX_ADDR_R/W (TX.ST bit 3) indicates whether the NEURON CHIP is reading or writing a transceiver register. TX_ADDR_R/W=0 indicates a write; TX_ADDR_R/W=1 indicates a read. TX_ADDR_2-0 indicate one of seven possible registers, from 1-7 (bit 2 is MSB). Register 0 is not defined. A write to register 0 is the steady-state condition; a read of register 0 causes the transceiver to reset.

The transceiver is required to accept and respond to configuration commands and status requests only in the idle state, that is, when the transceiver is neither transmitting nor receiving.

Configuration Command

In order to write to a transceiver register (i.e., to send configuration data), a NEURON CHIP CPU writes eight bits of register data which are shifted out in TX.DATA bits 7-0. (Bit 7 is the MSB and is shifted out first.) The NEURON CHIP CPU also sets TX_ADDR_R/W=0 (write) and TX_ADDR_2-0=1-7 (register number, bit 2 is MSB) which is the indication that the TX.DATA field of that frame contains the configuration byte. The transceiver acknowledges that the configuration is complete by asserting RD/WR_ACK (RX.ST bit 1) in the next frame. The write register command will be sent in consecutive frames at least until the transceiver acknowledges the command, and the command will be sent for an indeterminate number of frames after the response until a NEURON CHIP CPU clears the latches. The transceiver acknowledges each write command by asserting RD/WR_ACK in the following frame.

The NEURON CHIP firmware writes all of the possible configuration registers in descending order, from register 7 to register 1. However, if the transceiver uses fewer than the maximum number of 7 registers, full address decoding is not required; if the transceiver uses the registers in ascending order, the subset of the registers that are actually implemented on the transceiver will be the last ones written to, and thus contain the correct values.

The transceiver must provide a RD/WR_ACK for configuration of each of the seven registers, regardless of how many registers actually are implemented on the transceiver. The RD/WR_ACK from the transceiver is issued in the frame following the configuration command.

Bit 7 of configuration register 1 is always required. This configuration bit, referred to in the following sections as ALT_PATH, indicates which of two possible transmission modes to use. These transmission modes are dependent on the transceiver design, and more than one mode need not be implemented by the transceiver designer. Examples of transmission modes are the following: two different speeds, two different channels or carriers, or a combined speed and carrier frequency change. The NEURON CHIP firmware will switch back and forth between these two alternatives prior to transmitting a packet under normal operation, so the modification of this configuration bit cannot disrupt the operation of the transceiver. The change over from ALT_PATH = 1 to ALT_PATH = 0 or from ALT_PATH = 0 to ALT_PATH = 1 must occur in 1 frame.

It is the transceiver implementer's choice as to whether this capability of multi-channel or multi-speed capability is to be implemented, but if the transceiver designer does decide to implement this feature, it is required that that the transceiver be designed to detect carrier on both paths simultaneously, and be able to receive a packet on either channel without any configuration action by the NEURON CHIP. For example, a transmitting NEURON CHIP may decide to initiate a re-try message at a lower data rate. All the other transceivers must be able to detect that slower message on the channel and adapt their receivers to receive the packet without any configuration action on the part of the NEURON CHIPs attached to the transceivers which are receiving the slower packet. The same holds true if, instead of speed, the carrier frequency, modulation technique, etc. is changed by selecting the ALT_PATH configuration bit.

In no case is it required for the transceiver to be able to receive two simultaneous messages, one on each of the alternate paths. The upper layers of the protocol attempt to make it so that this condition occurs infrequently. When this condition occurs, it is a collision, and it is acceptable that the transceiver receives either one or none of the colliding packets.

Whenever the ALT_PATH function is implemented in the transceiver, ALT_PATH = 1 is understood by the NEURON CHIP firmware to be the more reliable and is used as the "last resort" to get a packet through the network.

Status Request

In order to read a register (request status data), a NEURON CHIP CPU sets TX_ADDR_R/W=1 (read), and TX_ADDR_2-0=1-7 (register number, bit 2 is MSB). The transceiver returns the status byte by shifting out the byte in

the field RX.DATA bits 7-0. (Bit 7 is the MSB and is shifted out first.) The transceiver asserts RD/WR_ACK to indicate the register contents are available in RX.DATA bits 7-0 of the same frame. The read register command will be sent in consecutive frames at least until the transceiver acknowledges the command and returns the status byte, and the command will be sent for an indeterminate number of frames after the response until a NEURON CHIP CPU clears the latches. The transceiver responds to each read command by returning the contents of the status register and asserting RD/WR_ACK in the frame following the command.

The transceiver must provide a RD/WR_ACK for a status request of any register, 1 through 7, regardless of the actual number of status registers implemented on the transceiver. The status registers are read as a result of the node receiving a network management command to do so. It is assumed that the node issuing the network management command knows which registers are implemented, and what the status registers mean. The RD/WR_ACK is issued in the frame following the status request command, such that the status byte is in the same frame as the RD/WR_ACK.

Handshaking Diagrams

Figures 2-8 illustrate the handshaking that occurs between the NEURON CHIP and transceiver for different scenarios, as described in the text above. In the diagrams, each pair of arrows represents the exchange during one frame. The status field from the NEURON CHIP to the transceiver, TX.ST, is on the upper arrow; the status field from the transceiver to the NEURON CHIP, RX.ST, is on the lower arrow. The values of the status fields are written in hexidecimal, with the key bit values in parentheses. The transceiver states on the right side refer to the state diagram following. In each scenario, the transceiver begins and ends in the IDLE state.

State Diagram

Figure 9 shows an example of a state diagram for a transceiver using the special-purpose mode interface. For each state transition, the label has format "input that caused the transition/resultant output." The input may either be bits of the TX.ST field from the NEURON CHIP, network status, or internal transceiver conditions. The resultant output is the RX.ST field to the NEURON CHIP.

Reset

The NEURON CHIP's external reset output is tied to the transceiver's reset input and causes the transceiver to reset its state and internal registers. The transceiver is no longer configured after the reset signal causes a hard reset. Upon a hard reset of the transceiver, all configuration information is lost. The NEURON CHIP will then download the configuration registers in descending order. During this time, that is, until configuration register 1 is written, the transceiver must not receive and forward incoming packets to the NEURON CHIP and the transceiver must reject any requests from the NEURON CHIP to transmit.

In addition, the NEURON CHIP may issue a soft reset command by setting TX_ADDR_R/W=1 and TX_ADDR_2-0=0. If the transceiver is in any state but IDLE and the NEURON CHIP issues this soft reset command, the transceiver aborts whatever it is doing and returns to the IDLE state. The soft reset does not cause the transceiver to reset its internal registers; the transceiver remains configured after the soft reset command.

The NEURON CHIP Handshake Timing

The following timing parameters are a function of the NEURON CHIP input clock period and the interface bit clock period. The notation icp refers to the input clock period and bcp refers to the interface bit clock period

Maximum time between SET_TX_FLAG and first TX_DATA_VALID *	732 icp + 27 bcp
Maximum time between TX_DATA_CTS and TX_DATA_VALID	15.5 bcp
Minimum time between consecutive assertions of TX_DATA_CTS	16 bcp
Maximum time between last TX_DATA_VALID and TX_FLAG reset	14 bcp
Minimum time between RX_FLAG set and first RX_DATA_VALID*	1380 icp - 11 bcp
Minimum time between consecutive assertions of RX_DATA_VALID	16 bcp
Minimum time between RD/WR_ACK set and RX_FLAG set	31 bcp

*This parameter affects the minimum duration of the transceiver's preamble.

Transceiver-Specific Items

Function

Items that are to be defined by a specific transceiver include:

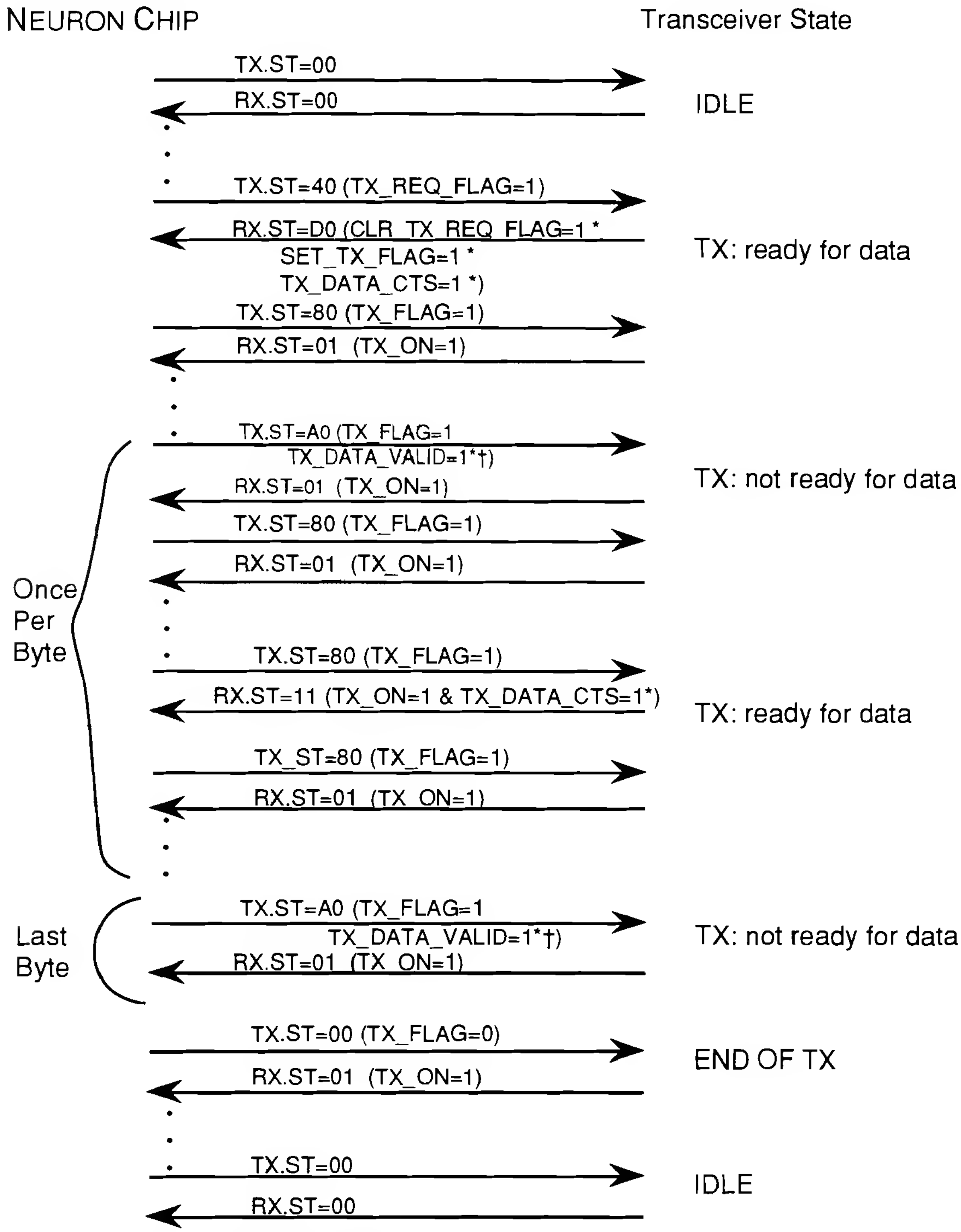
- Definition of the registers that the NEURON CHIP may read and write
- Definition of preamble

- Use of watch-dog timers on the transceiver (e.g., such that the node does not fail in a way that ties up the network indefinitely)
- Use of transceiver sleep modes

Timing

Refer to the section "Specifying Custom Transceiver Types" in the *LONBUILDER User's Guide* for parameters to build a network of special-purpose mode transceivers.

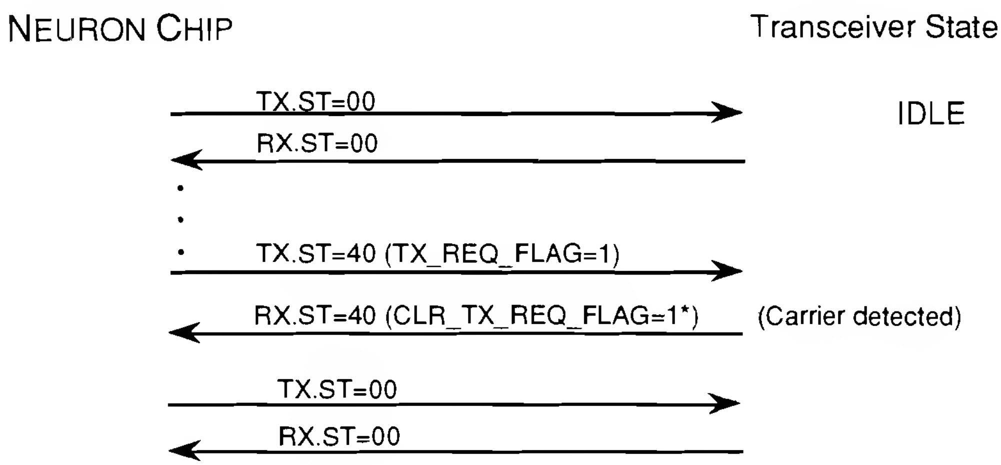
Figure 2. Transmit Sequence: Packet Sent



* Status bit asserted for one frame only.

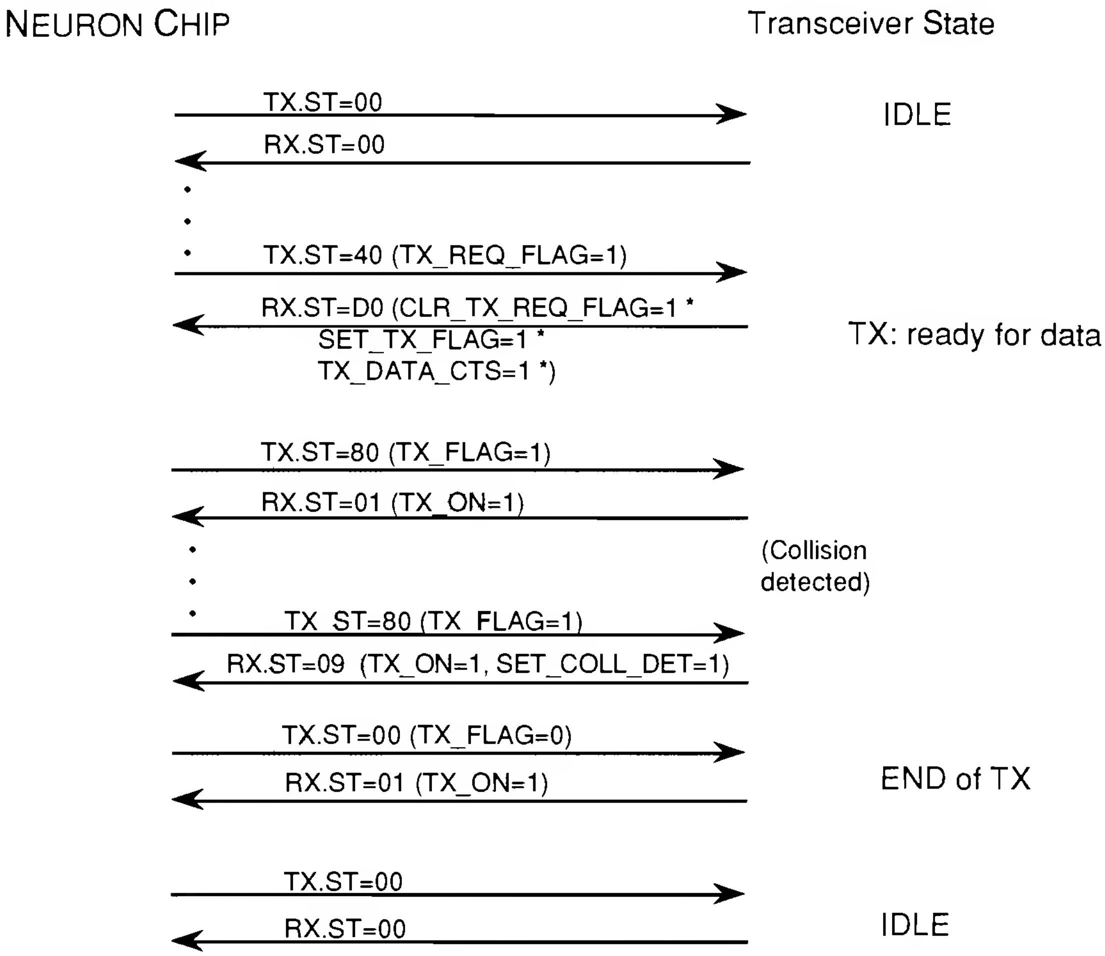
† Following TX.DATA field (same frame) contains valid data.

Figure 3. Transmit Sequence: Collision Avoidance



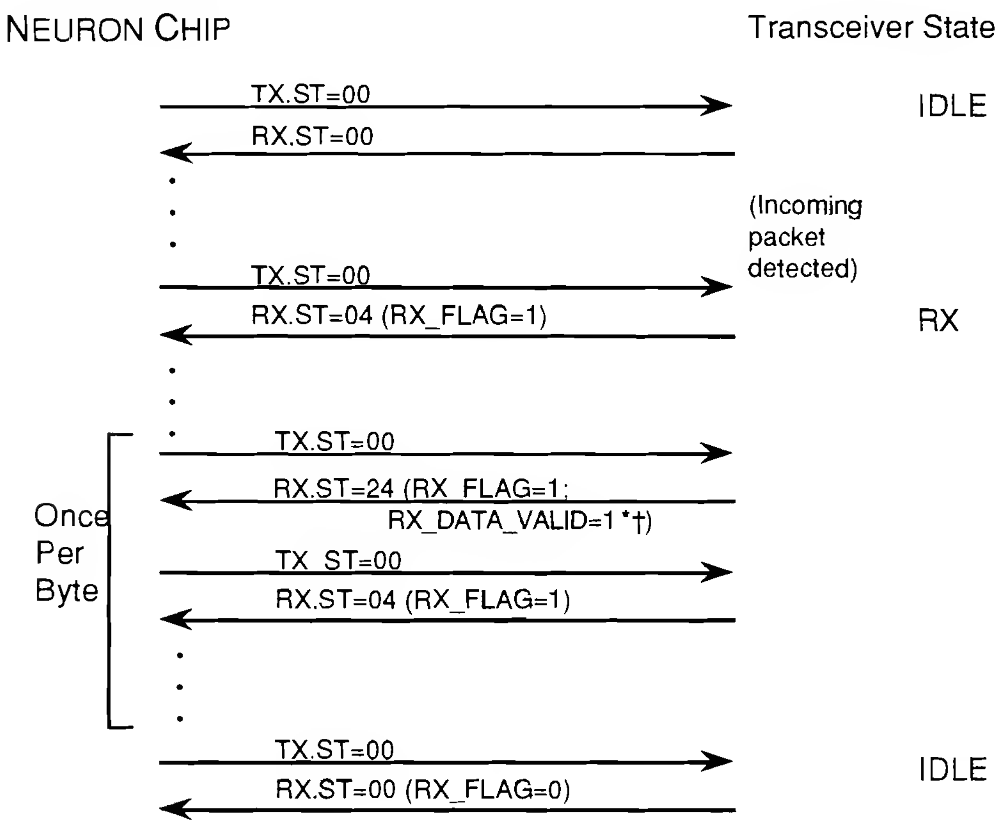
* Status bit asserted for one frame only.

Figure 4. Transmit Sequence: Collision



* Status bit asserted for one frame only.

Figure 5. Receive Sequence



* Status bit asserted for one frame only.

† Following RX.DATA field (same frame) contains valid data.

Figure 6. Receive Sequence: Error (i.e. no bit sync)

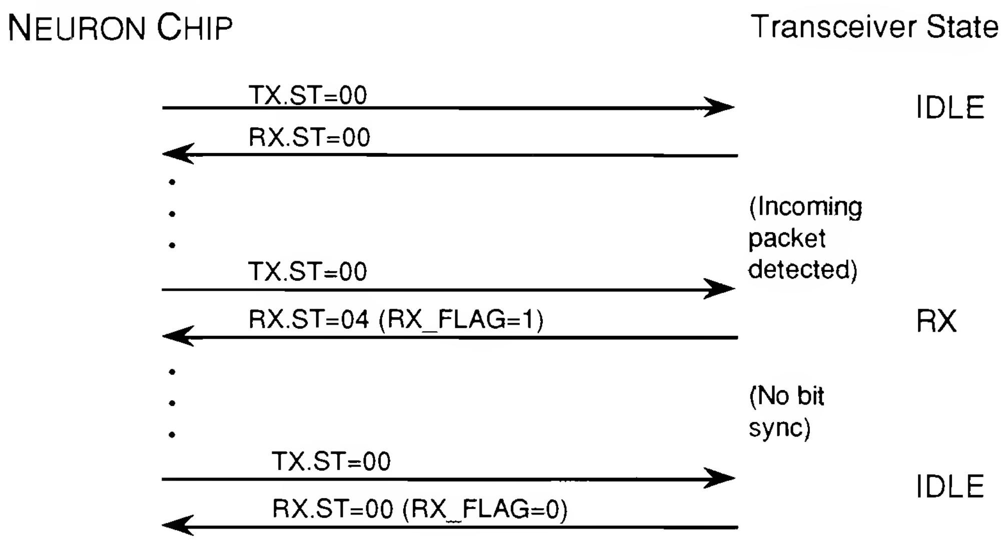
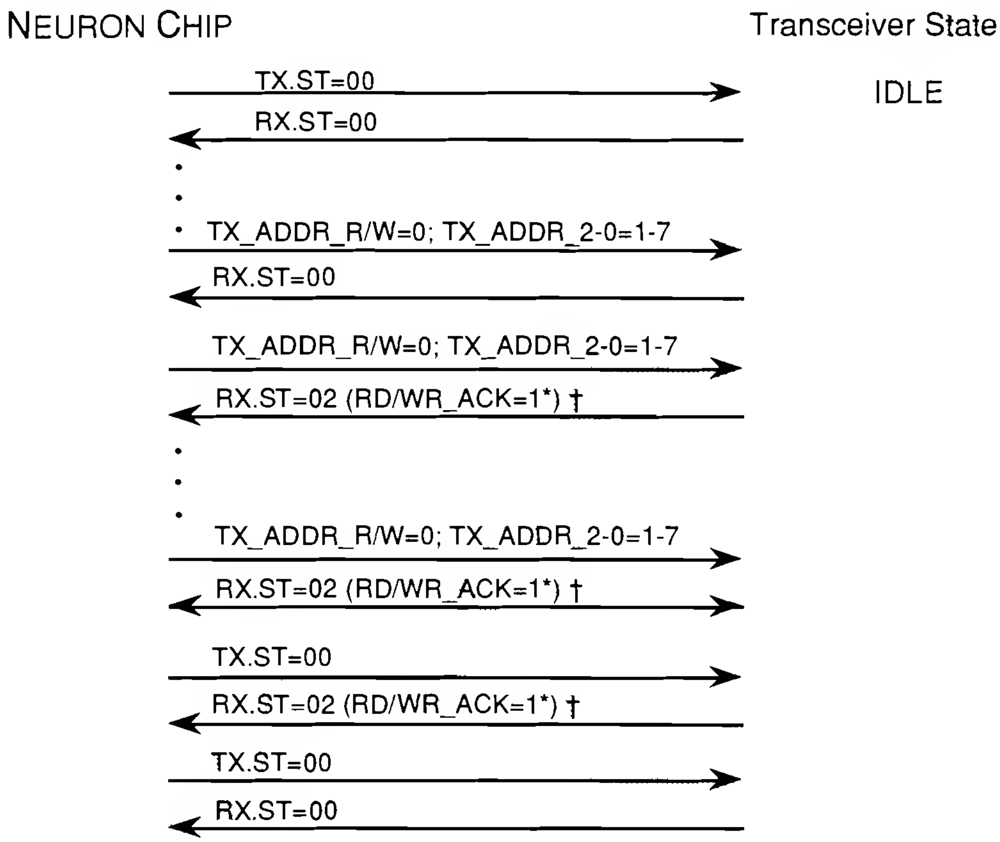


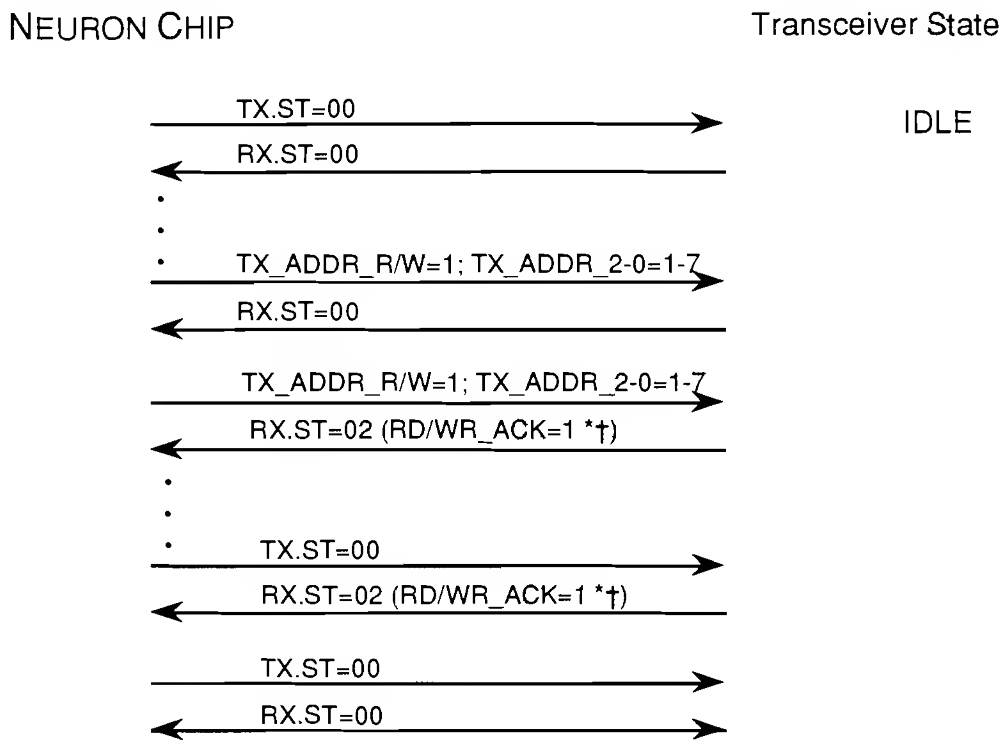
Figure 7. Configuration Command Sequence



* Status bit asserted for one frame only.

† Following TX.DATA field (same frame) contains valid configuration byte.

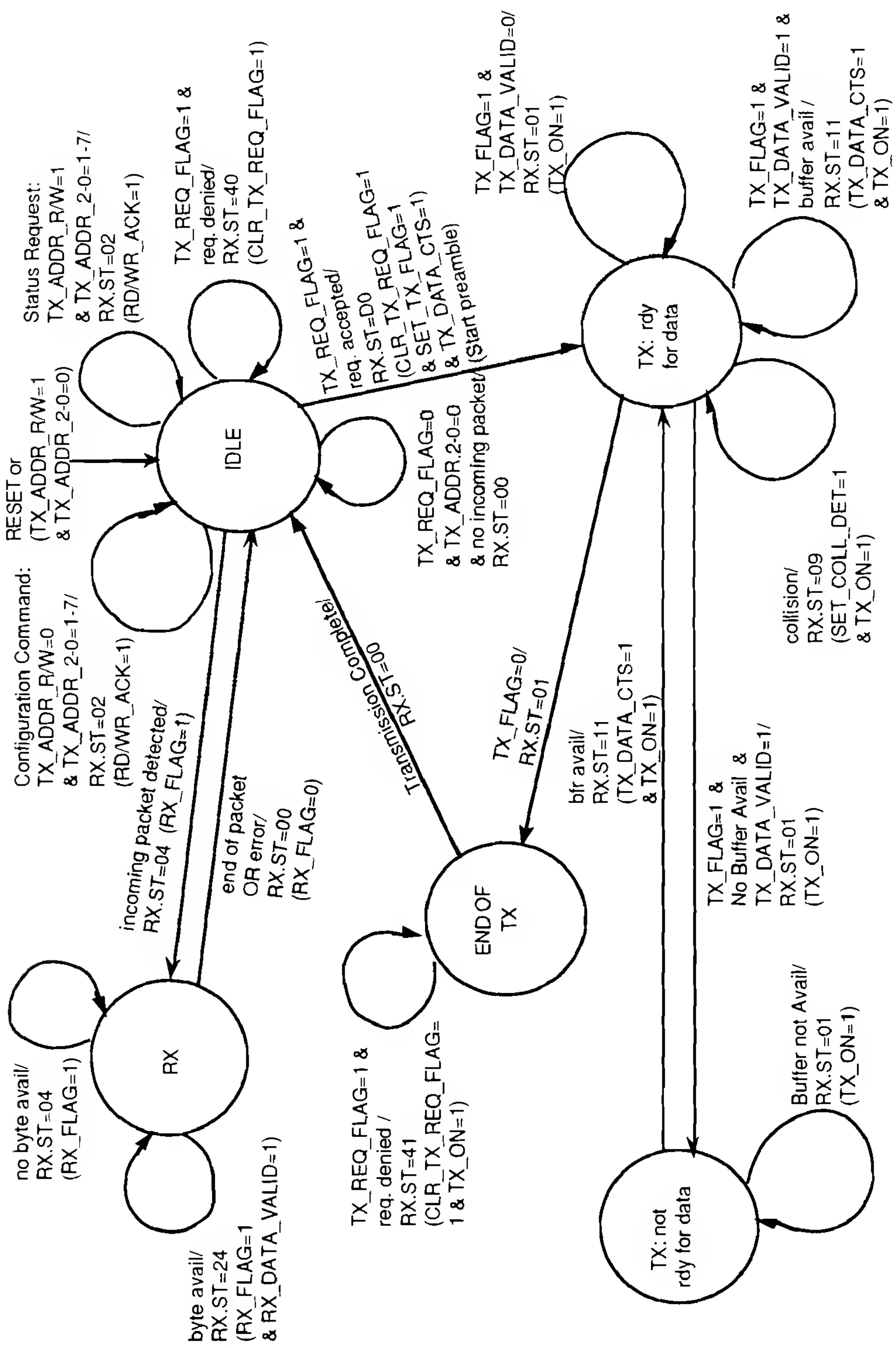
Figure 8. Status Request Sequence



* Status bit asserted for one frame only.

† Following RX.DATA field (same frame) contains valid status byte.

Figure 9. Example Transceiver State Diagram



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